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1. (amended) A method for calculating an orthogonal discrete transform on the basis of the DIT method in prescribed intermediate steps,

wherein

a) the data are read from a memory [(1)] organized on a page-for-page basis,

b) the intermediate step prescribed by the transform is carried out,

c) the resulting data are stored in a buffer memory [(5)], and

d) the resulting data are written page-for-page from the buffer memory [(5)] to the memory [(1)] organized on a page-for-page basis.

2.(amended) A method for calculating an orthogonal discrete transform on the basis of the DIF method in prescribed intermediate steps,

wherein

a) the data are read from a memory [(1)] organized on a page-for-page basis,

b) the data are stored in a buffer memory [(5)],

c) the intermediate step prescribed by the transform is carried out, and

d) the resulting data are written page-for-page from the buffer memory [(5)] to the memory [(1)] organized on a page-for-page basis.

3.(amended) A method for calculating an orthogonal discrete transform on the basis of the DIF method in prescribed intermediate steps,

wherein

the data are read from two memories [(3, 4)] organized on a page-for-page basis, such that the reading is organized on a page-for-page basis, the intermediate step prescribed by the transform is carried out, and

the resulting data are again written page-for-page to the two memories [(3, 4)] organized on a page-for-page basis.

4.(amended) The method as claimed in [one of claims 1 to 3] claim 1, wherein the discrete orthogonal transform is formed by an FFT, IFFT, DCT or IDCT.

7.(amended) An apparatus for carrying out the method as claimed in [one of claims 1, 4, 6] claim 1

wherein

the apparatus has a memory [(1)] organized on a page-for-page basis, a processor [(2)] and a directly organized memory [(5)] which is arranged downstream of the processor.

8.(amended) An apparatus for carrying out the method as claimed in [one of claims 1, 4, 6] claim 1

wherein

the apparatus has a memory [(1)] organized on a page-for-page basis, a processor [(2)] and a directly organized memory [(5)] which is arranged upstream of the processor.

9. (amended) The apparatus as claimed in [one of claims 7 or 8] claim 7, wherein the page-oriented memory [(1)] is a large memory in relation to the directly organized buffer memory [(5)].

10.(amended) The apparatus as claimed in claim 9, wherein a fast memory is used for the buffer memory [(5)].

11.(amended) The apparatus as claimed in [one of claims 7-10] claim 7, wherein the page-oriented memory [(1)] is a dram and buffer memory [(5)] is an SRAM.

12.(amended) The apparatus as claimed in [one of claims 7-11] claim 7, wherein the page-oriented memory [(1)] has a size of 8 K addresses and the buffer memory [(5)] has a size of 32 - 64 addresses.

13.(amended) An apparatus for carrying out the method as claimed in [one of claims 3, 4-6] claim 3

wherein

the apparatus has two memories [(3, 4)] organized on a page-for-page basis and a processor [(2)].

14.(amended) The apparatus as claimed in claim 13, wherein the page-oriented memories [(3, 4)] are of the same size.

15.(amended) The apparatus as claim in claim 14, wherein the page-oriented memory [(3, 4)] has a size of 4 K addresses.

16.(amended) The apparatus as claimed in [one of claims 7-15] claim 7, wherein the processor [(2)] provides a Butterfly.